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ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

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FORWARD

The research covered in this report is carried out in a team effort having the Rockwell International Electronics Research Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred A. Blum. The principal investigators for each organization are:

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TECHNICAL SUMMARY

This report covers the third quarter, Phase II, of a program on ion implanted planar GaAs digital integrated circuit technology. The goal for Phase II of the program is to achieve the capability of fabricating GaAs ICs of LSI complexity. The fabrication approach, demonstrated in Phase I, is based on multiple localized implantations directly into the semi-insulating GaAs substrate to form active device areas insulated by the unimplanted regions of the substrate. The circuit concept, also demonstrated in Phase I, involves a combination of Schottky diodes and depletion mode Schottky barrier FETs (SDFL), employed to form logic gates capable of high speed operation with very low power.

This program requires a research effort on all the multiple facets of process development. The research activities range from substrate growth and ion implantation technology to fabrication and evaluation of test circuits. These activities are carried out by the Electronics Research Center with the support of three subcontractors, Caltech, Cornell University, and Crystal Specialties, Inc.

The most important aspects of the work carried out in this quarter were gaining of further insight into the causes for conversion of unqualified GaAs substrates, the fabrication of wafers with mask set AR3, and the preparation for evaluating the 3 x 3 parallel multiplier, a new circuit on AR3. This circuit will provide vital information for the design of the more complex circuits on mask set AR4.

The following is a summary of the accomplishments of the program in the past quarter.

Semi-insulating Substrate Material (Sec. 2)

Evaluation by SIMS of the redistribution of chromium during annealing has continued. The electrical measurement of doping tails on Se implanted layers in unqualified substrates resulted in shallow donor and Cr profiles which have correlated well with bulk Cr density profiles obtained from SIMS data. The results support the model, proposed in the previous report, attributing the formation of an n-type layer in unqualified substrates to lack of compensation of shallow donors due to Cr depletion. Efforts were initiated at Crystals Specialties to reduce the background donor concentration in the bulk material. A protective coating of Si_3N_4 on the growth boat has been applied. Since Si_3N_4 is more stable than SiO_2, and it does not wet as easily, decomposition of the growth boat should be reduced. Electrical evaluation of ingots grown by this technique is presently being carried out.

A decrease was observed in the incidence of inclusions in the grown material. This appears to have resulted from greater care in cleaning and handling of the growth boats. A clean room has been established for this purpose at Crystal Specialties.

Planar Process Development (Sec. 3)

Fabrication of wafers has continued without any major change in the direction of the process. Mask set AR3 has been extensively used for wafer fabrication. Several wafers have been completed, and are now under test. Further studies of silicon implantation for high doping have been carried out. Attempts to use Si-P implantations so that P forces Si into the Ga sites for higher activation have not been successful so far.

In wafer fabrication, the ion milling technique has totally replaced the previous lift-off procedure for the fabrication of the second layer metallization. Beam orientation effects on etch rates and metal redeposition have been studied in detail in order to determine the optimum beam direction.

Circuit Performance (Sec. 4)

Evaluation of processed wafers using the automatic test system has continued on a routine basis, as a complementary step of the fabrication process. Doping profiles are also measured on chip by the automatic system using the C-V technique. A successful measurement of mobility profiles was recently accomplished using a "fat FET" configuration. Mobilities higher than 4000 cm^2/Vs were measured. Averages from FETs statistics indicate that such mobility values are representative of most IC FET channel layers, with relatively small variations from wafer to wafer.

The strategy for testing the new 3 x 3 parallel multiplier circuit on wafers fabricated with mask set AR3 has been layed out, and measurements are in progress. Further refinement on the FET analytical model developed at Cornell University have been introduced. These refinements consist mainly on a hybridization of the previous model with the Shockley model at gate voltages near threshold, resulting in an improved fit with I-V characteristics of test FETs on IC wafers.

1.0 INTRODUCTION

This report covers the third quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The objective of this program is the development of an integrated circuit process technology for GaAs taking advantage of its superior electrical properties in order to achieve high speed low power digital integrated circuits. The goal for Phase I was to establish the technology, and demonstrate its viability by fabricating circuits reaching MSI complexity. The goal for Phase II is to achieve the capability of fabricating GaAs ICs of LSI complexity. The bulk of the work on this program is carried out at the Rockwell International Electronics Research Center. Significant assistance is provided by three subcontractors; Crystal Specialties Inc., California Institute of Technology, and Cornell University.

In the previous quarter, high speed data from wafers fabricated with mask set AR2 were reported, showing excellent high speed operation of a ripple divider, an 8-input data multiplexer, and an 8-output data demultiplexer. In this quarter wafers were processed to completion using mask set AR3, and the routine low frequency testing was performed. Preparations have been made for testing a new MSI circuit on mask set AR3, the 3 x 3 parallel multiplier, and measurements are now in progress. The results from these measurements, that will be reported in the next quarter, will provide vital guidelines for the design of the more complex circuits on mask set AR4.

Work on all other aspects of the program has continued. Evaluation (by SIMS) of the redistribution of Cr during annealing done on several different annealing caps indicate a dependence of the Cr profile on the As vacancy concentration. In addition, electrical evaluation of doping tails on Se implanted layers in unqualified substrates resulted in shallow-donor and Cr profiles which have correlated well with bulk Cr density profiles obtained from SIMS data. The results support our model, which attributes the formation of an n-type layer after annealing of unqualified substrates to lack of compensation due to Cr depletion.

As a result of the Cr redistribution analysis, efforts were initiated at Crystal Specialties to reduce the background donor concentration in the bulk material. A protective coating of Si_3N_4 on the growth boat has been applied. Since Si_3N_4 is more stable than SiO_2, and it does not wet as easily, decomposition of the growth boat should be reduced. Electrical evaluation of ingots grown by this technique is presently being carried out.

Optimization of the ion milling process for second level metal definition has continued. Etch rate and redeposition effects as a function of the angle of incidence have been evaluated. As a result, the ion milling method has been successfully used to fabricate wafers from mask sets AR2 and AR3 with excellent results.

Acquisition of capacitance-voltage profiles and calculation of doping profiles from PM test patterns has been carried out automatically on the low frequency probe station. Mobility profiles, using a "fat FET" test pattern on

PM, have also been measured, obtaining peak mobilities in excess of 4000 cm^2/Vs.

As mentioned above, wafers have been processed using mask set AR3 during the past quarter. Several wafers are presently being evaluated for high speed performance of MSI circuits. The 3 x 3 parallel multiplier containing 75 gates is the first new MSI circuit being tested. Automatic data acquisition methods will be used to evaluate the functional accuracy of this circuit under all combinations of input codes at low speeds. Propagation delay times will be evaluated using the ring oscillator feedback mode of this circuit.

The FET device modeling work at Cornell has been extended to include the shape of the ion implanted doping profile. It has also been hybridized with the Shockley model to improve the fit with experimentally determined I-V characteristics near threshold.

2.0 MATERIALS

The supply and characterization of semi-insulating GaAs substrates appropriate for use with ion implantation are areas of considerable importance to the long-term development of the planar GaAs IC technology. The efforts under this contract directed at improving the state-of-the-art in these areas include: bulk growth of semi-insulating GaAs (described in Section 2.1); evaluation of the performance of the semi-insulating substrates under ion implantation (described in Section 2.2); and further analytical work directed at an improved understanding of the behavior of the substrates (described in Section 2.3).

2.1 Growth of Semi-insulating GaAs (Crystal Specialties)

The activities at Crystal Specialties have been directed towards improving the yield of ingots having high crystalline perfection, high resistivity, and that are qualified for use in the ion-implantation process. During this quarter, the fraction of growth runs yielding single crystals and the fraction of Cr doped single crystal ingots which yielded high resistivity material were both maintained at good levels (53% and 86%, respectively). As reported more fully in Section 2.2, the qualification yield was also good (66%), however this number was obtained on the basis of a small number of ingots. A decrease was observed in the incidence of inclusions in the grown material. This appears to have resulted from greater care in cleaning and handling of the growth boats. A clean room has been established to ensure a high level of cleanliness during the ampoule-loading phase of the growth process.

The analytical work described last quarter[1] suggested that the difficulties encountered in unqualified semi-insulating GaAs ingots (which include surface conversion and the formation of deep tails in donor implant profiles) are caused, at least in part, by residual donor concentrations in the ingots. As a result of Cr redistribution during post-implant annealing, the residual donors become under-compensated, and contribute extra carriers at the sample surface. The analytical work suggested that if the donor concentration could be maintained at a low enough level, then the material would be free of these problems. Based on this analysis, work was initiated to reduce the background donor concentration in the material. The presence of donors has been widely attributed to the incorporation of Si, which originates from decomposition of the quartz used as the growth boat and surrounding ampoule. One method that is being pursued to reduce this contamination is to apply a protective coating of Si_3N_4 to the growth boat. Since the energy of formation of Si_3N_4 is higher than that of SiO_2, and since Si_3N_4 is more stable than SiO_2 to the action of molten metals, it is expected that the decomposition of the growth boat will be reduced. To date, several ingots of GaAs have been grown in boats prepared in this manner. The results have been encouraging inasmuch as the occurrence of boat-wetting was at least as low as the level obtained in the uncoated boats. Electrical evaluation of the grown ingots is currently being carried out. Similar protection of the walls of growth ampoule has not yet been implemented, but may prove to be necessary.

2.2   Substrate Evaluation (Electronics Research Center)

To evaluate the performance of semi-insulating GaAs ingots under the ion-implantation process, the test based on Kr ion implantation (followed by capping and annealing), the isolation test (capping and annealing without implantation) and examination of carrier density profiles for representative FET channel implants were continued. These tests were performed on 3 ingots grown by Crystal Specialties, of which 2 were found fully qualified for ion-implantation (type A). This represents an increase in qualification yield over values typically obtained in the past, but sampling of larger number of ingots is required to confirm this result.

Similar evaluation was done on 7 ingots grown by Mitsubishi-Monsanto. The results indicated that 2 ingots (29%) were qualified, although they displayed relatively deep carrier profiles following implantation (and are thus classified as type B ingots).

2.3   Analysis of Semi-insulating GaAs (Electronics Research Center)

The photoinduced transient spectroscopy technique (PITS) described in previous reports has been used further to investigate electrically active point defects found in the as-grown substrates, as well as centers introduced during processing. The theoretical framework for quantitative estimation of defect concentrations is presently being developed. Initial results indicate that the electron trap with activation energy 0.26 eV and characteristic PITS temperature T_m = 202K previously observed in most of the substrates (see

Quarterly Technical Report No. 7)[1] is present in at least some of the samples in very high concentrations, $\sim 10^{17}$ cm^{-3}. This trap has a dominant effect on the temperature-dependent photoconductivity characteristics and thermally stimulated current behavior of the samples. The observed concentrations of this level are greater near the front of ingots, suggesting that it is associated with an element with distribution coefficient of order unity. Its small capture coefficient for electrons ($S_n \sim 10^{-16}$ cm^2) suggests that it is acceptor like (although it lies in the upper half of the bandgap). This trap decreases in concentration upon annealing at 850°C. These properties are similar to those postulated by Weiner and Jordan for the Si-O complex invoked to explain compensation and anneal behavior in undoped GaAs.[2] Traps of this density may be expected to have a pronounced effect on the compensation of implanted donors, and further investigation of this defect appears worthwhile.

The use of the SIMS technique to explore the redistribution of Cr during the anneal phase of the IC process has continued. It has been found that Cr migration, leading to a depletion of Cr near the surface, occurs in substrates annealed without a cap, and in substrates annealed with Al and SiO$_2$ caps, as well as with the Si$_3$N$_4$ caps studied earlier. Differences in the resulting shape of the Cr profile were seen in the capless and Al capped case, however. This tends to indicate an influence of arsenic vacancy concentration on the Cr diffusion coefficient. The detailed nature of the driving force for the Cr motion is currently unknown. It has been suggested (by L. Eastman of Cornell University) that the underlying cause is the low Cr solubility in GaAs at the anneal temperature.

The understanding of the role of Cr redistribution in the formation of deep tails of free carriers in Se implanted unqualified substrates has led to an electrical technique for the measurement of residual donor concentrations (N_d) and chromium concentrations (N_{Cr}) in the Se samples. Both concentrations can be derived from extrapolations of the carrier density vs depth measured in the tail region. For example, Fig. 2.3-1 shows carrier density profiles for a number of Se implanted unqualified ingots. The extrapolated value at x = 0 of the linear component of extra carriers may be interpreted as the residual net donor concentration N_d. The values of N_d have typically been found to be of the order of 10^{16} cm^{-3}, which coincides with typical electron concentrations in ingots grown without Cr. Additionally, the bulk Cr concentration may be derived from the slope of the carrier density in the tail region, since

$$\frac{dn}{dx} \simeq - \left[\frac{dN_{Cr}(x)}{dx} \right]_{x=0} = - \frac{N^0_{Cr}}{2\sqrt{Dt}}$$

The value $\sqrt{Dt}$ = 1.25 µm, found for Cr redistribution in Si$_3$N$_4$ capped samples annealed at 850°C for 30 min, was used to infer values of bulk Cr concentration for unqualified ingots obtained from a number of suppliers. Table 2.3-1 shows the good correlation found between values of N_{Cr} obtained in this manner with values obtained by SIMS and from manufacturers specifications (based on the amount of Cr added to the melt).
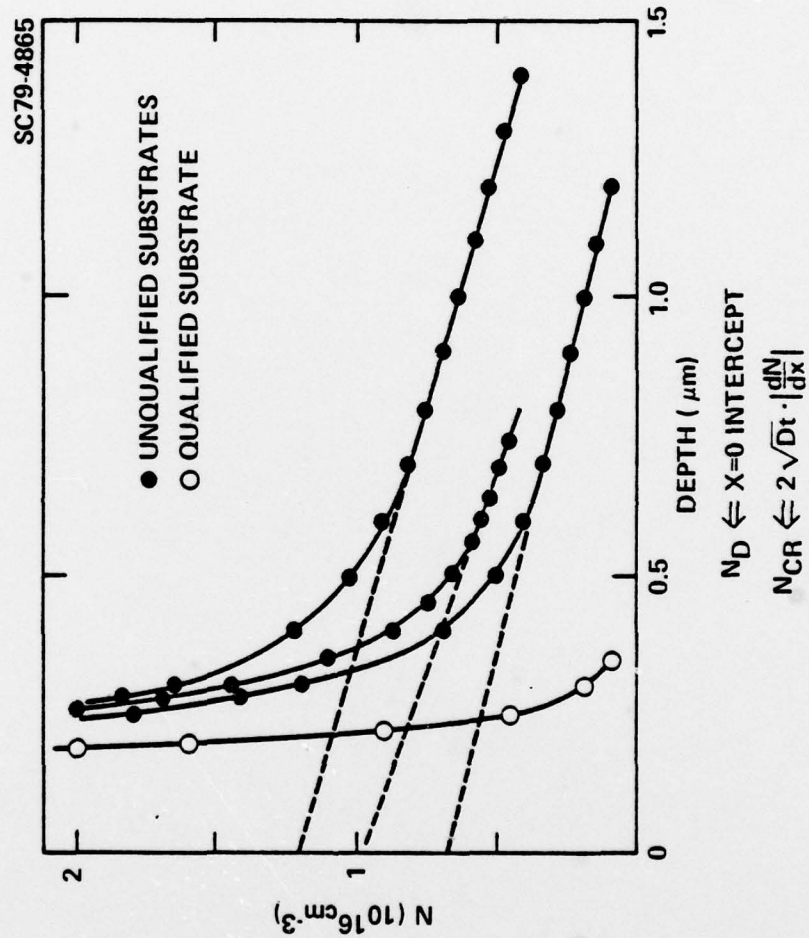
Fig. 2.3-1 Carrier density vs depth measured for Se implanted, annealed samples, shown on a scale which emphasizes the tail region.

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TABLE 2.3-1

Bulk Cr Concentration in Unqualified Ingots
Measured With Various Techniques

Sample	Electrical	SIMS	Growth Data
A	2.0×10^{17}	1.8×10^{17}	1.6×10^{17}
B	4.9×10^{16}	4.2×10^{16}	Not Available
C	1.9×10^{16}	3.8×10^{16}	$\sim 1.9 \times 10^{16}$
D	1.8×10^{16}	2.7×10^{16}	$\sim 1.9 \times 10^{16}$

It was confirmed by C-V measurements on samples whose bulk chromium concentration was known that as a result of the Cr redistribution the characteristics of Se implanted layers (such as used in the FET channels) were largely insensitive to N_{Cr}. This result establishes the beneficial aspect of the observed Cr redistribution in that it "getters" the chromium from the implanted region.
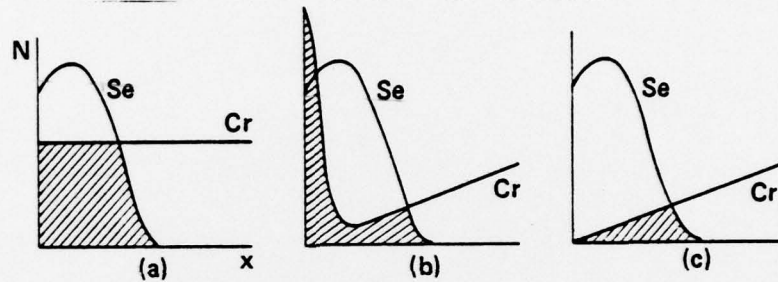
In particular, the concentration of Cr incorporated into semi-insulating GaAs typically varies between wide limits. Such variation is difficult to avoid since Cr density gradients occur within a given ingot due to the low Cr segregation coefficient, and since no convenient method currently exists to classify grown slices according to Cr content. In light of this, one must in principle be concerned that (qualified) semi-insulating substrates will be overcompensated to a variable extent, and that as a result, the activation of donor implants will vary unpredictably from substrate to substrate. This hypothetical problem does not seem evident in practice, however. It is reasonable to believe that as a result of Cr outdiffusion, the implanted region contains a low Cr concentration, nearly independent of the bulk Cr density. This effect is shown schematically in Fig. 2.3-2 (a) and (c).

An additional possibility must be considered, however. The SIMS data tend to suggest that an accumulation layer forms over a region as much as 1000A wide. In this region the Cr density could attain very sizeable values, since it could contain the Cr content initially distributed over several microns (total sheet concentration of the order of 5×10^{12} cm^{-2}). Such a

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$$V(W_o) = \frac{q}{E} \int_0^{W_o} \eta(x) x \, dx$$

$$\eta(x) = N_{Se}^+(x) \cdot N_{Cr}^- + [N_D^+ \cdot N_A^-]$$

APPLIED VOLTAGE TO DEPLETE 1200A
Se IMPLANT - $2.5 \times 10^{12} cm^{-2}$ - 400 KeV
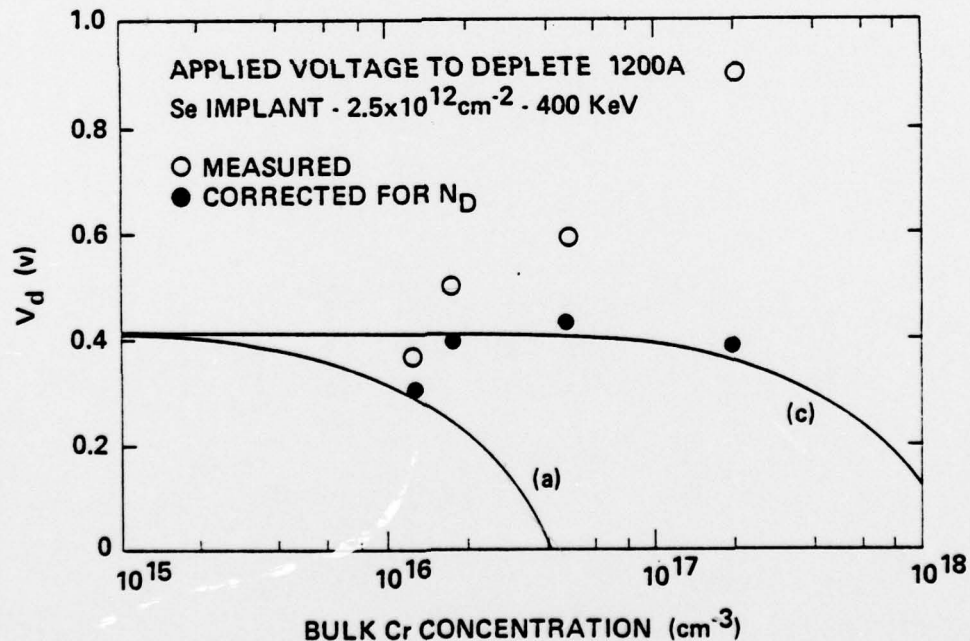
○ MEASURED
● CORRECTED FOR N_D

Fig. 2.3-2 Schematics of several possibilities for the effect on Cr redistribution on the depletion voltage of ion implanted layers: (a) no Cr redistribution; (b) redistribution with electrically active Cr accumulation region; and (c) Cr redistribution without electrically active accumulation layer. Also shown are data points corresponding to the measured voltage required to deplete 1200Å in Se implanted, unqualified substrates of varying bulk Cr concentration, showing agreement with case (c).

region might be expected to have an appreciable effect on the properties of implanted layers, as shown schematically in Fig. 2.3-2 (b). An attempt to distinguish experimentally between the three possibilities was undertaken using samples whose Cr and residual donor concentrations were known via electrical measurements (which required the use of unqualified substrates). The region within 1000A of the surface, unfortunately, is not conveniently accessible for C-V profiling due to depletion from the built-in voltage of the Schottky diodes. To obtain a measure of the carrier concentration in this region, the applied voltage necessary to deplete the surface to a fixed depth (chosen to be w_o = 1200A) was used; this provides a weighted average of the carrier density (after taking into account the built-in potential), according to

$$V_T(w_o) = V_{bi} + V_d(w_o) = \frac{q}{\varepsilon} \int_o^{w_o} N(x) \; x \; dx$$

Figure 2.3-2 shows experimental values of V_d as a function of bulk Cr concentration in the substrates. After correction for the residual donor concentration in the samples (which was large since the substrates were unqualified), it was found that V_d was approximately independent of Cr concentration. This result confirms the expected effect of Cr gettering. In addition, it establishes that any voltage contribution of the Cr accumulation region (although not completely ruled out) is at least small enough not to produce untenable shifts in pinchoff voltage in FETs.

3.0 PLANAR PROCESS DEVELOPMENT

Fabrication of wafers has continued without any major change in the direction of the process. Mask set AR3 has been extensively used for wafer fabrication. Several wafers have been completed, and are now under test. Further studies on Si implantation have been carried out, and are reported in Sec. 3.1. The ion milling technique has totally replaced the previous lift-off procedure for the fabrication of the second layer metallization. Beam orientation effects on the results of the ion milling process have been studied in detail. Results are presented in Sec. 3.2.

3.1   Ion Implantation (Caltech and Electronics Research Center)

Previous studies[3] of Si-implanted, Cr-doped, semi-insulating GaAs crystals have shown that the maximum attainable free electron concentration after furnace annealing was $2 \times 10^{18}/cm^3$, independent of implanted dose or annealing temperature. During the past quarter, double implantations of Si and P have been carried out to see if the electrical activity could be enhanced in this way. 100 keV Si or Si and P ions (same dose per ion species) were implanted at room temperature into GaAs substrates as described above. After capping and furnace annealing for 30 min in H_2, the samples were prepared for electrical depth profiling at Rockwell International. Initial Van der Pauw measurements on the surface had indicated that at an implanted dose of $2 \times 10^{13}/cm^2$, the sheet electron concentration, N_s, was about the same for the two implant conditions for annealing temperatures between 800 and 900°C. At an implanted dose of $10^{15}/cm^2$,

the samples implanted with both Si and P (total dose 2 x 10^{15}/cm^2) showed a ~ 50% higher sheet electron concentration than those implanted with 10^{15} Si/cm^2 only, for annealing temperatures of 800 and 850°C. Electrical stripping measurements done at Caltech on samples annealed at 850°C have shown that the net electron concentration reached a maximum of about 6 x 10^{17}/cm^3 and 8 x 10^{17}/cm^3 for 2 x 10^{13} Si/cm^2 and for 2 x 10^{13} Si/cm^2 and 2 x 10^{13} P/cm^2 implanted samples, respectively. The maximum concentration expected from LSS range theory in the case of 100% activation for implanted Si of 2 x 10^{13}cm^{-2} dose, would be 1.8 x 10^{18}/cm^2. The electron concentration profiles are rather flat in the first 3000A, the maximum corresponding roughly to the maximum predicted from LSS theory for the atomic concentrations. The electron mobilities have a value of approximately 3000 cm^2/Vs at the surface, decreasing monotonically with depth.

In the case of 10^{15}/cm^2 implants, the maximum electron concentration is 1.5 - 2 x 10^{18}/cm^3 for both single- and double-implanted samples, and occurs beyond the LSS range. The mobilities show a behavior similar to that observed in the lower dose implantations.

In summary, for the doses of Si and P chosen, initial observations do not show a significant change in the free electron concentration due to double implantation.

Further work on this project is in progress.

3.2 Multilevel Interconnect Process (Electronics Research Center)

Ion milling instead of lift-off is now used in defining the second-level interconnects. Because of the basic nature of a lift-off technique, it

had required to limit the metalization and Si_3N_4 thicknesses to 3000A in order to ensure high yield.[1] With the ion milling technique a 300/5000A Ti/Au layer and a 5000A Si_3N_4 layer can be used without affecting the yield. A thicker Si_3N_4 film has the advantage of reducing the cross over capacitance of the metalization overcrossings, while a thicker metal layer reduces the resistance of the interconnect lines and increases the current carrying capacity of the power buses.

As described in the previous report,[1] the second layer interconnect process sequence, using plasma deposited Si_3N_4, starts after completion of first level interconnects, once the devices and circuits are dc tested and the wafer receives a "process go" decision. The wafer is cleaned with a low energy O_2 plasma in order to remove any organics and to prepare the surface for adherence of the plasma Si_3N_4 film. A 5000A layer of Si_3N_4 is deposited on the GaAs ICs at a temperature of ~300°C. A photoresist pattern defines the via window openings that are required for connecting the first level interconnects to the second level interconnects. Via windows are plasma etched through the Si_3N_4 down to the underlying Au interconnect which serves as an automatic etch stop. The via window step is followed by the evaporation of second level interconnect metal and by a photolithography step to define the desired pattern of second level interconnect. The mask used for this step in the ion milling process is the inverse of the mask used in the lifting process. After the photoresist pattern is formed the unwanted portion of metal film is removed by ion milling. The circuit fabrication is completed by removing the remaining photoresist.

Angle of incidence is an important parameter in ion milling. It can
be selected to give either the maximum etch rate or the maximum differential
etch rate for a particular pair of materials. The latter is chosen for the IC
fabrication process, the etch ratio of Au to Si_3N_4 being maximum at 90° angle
of incidence.[4] If this angle is selected, a short extra milling period, which
is necessary to ensure that the metals are completely etched through, does not
etch the Si_3N_4 film to any significant degree.

The angle of incidence cannot be freely chosen for maximum
differential etch rates because the net redeposition rate of the etched
materials also depends on the angle of incidence. Redeposition is often
observed along the edges of photoresist patterns, where ridges of the material
are left behind after the resist pattern is removed. The redeposited material
is undesirable because it could interconnect isolated regions, or it might
prevent complete coverage by a subsequently deposited layer. The material is
redeposited on the vertical sidewalls of the photoresist pattern at glancing
angle with respect to the incident ion beam. If a 90° incidence angle is used
for best etch stop (maximum differential etch rate) the redeposited material
forms ridges to the height of the photoresist. This is shown in a scanning
electron micrograph in Fig. 3.2-1.

One solution to the redeposition problem is to a tilt the ion beam.
An off-normal ion beam will etch away the material as it is redeposited on the
sidewall of photoresist pattern. When a suitable incidence angle is used, the
net redeposit rate can be zero, and a nearly vertical wall of the etched
pattern can be obtained. This is illustrated in Figs. 3.2-2(a), (b) and (c)
showing SEM photographs of samples etched at three incidence angles

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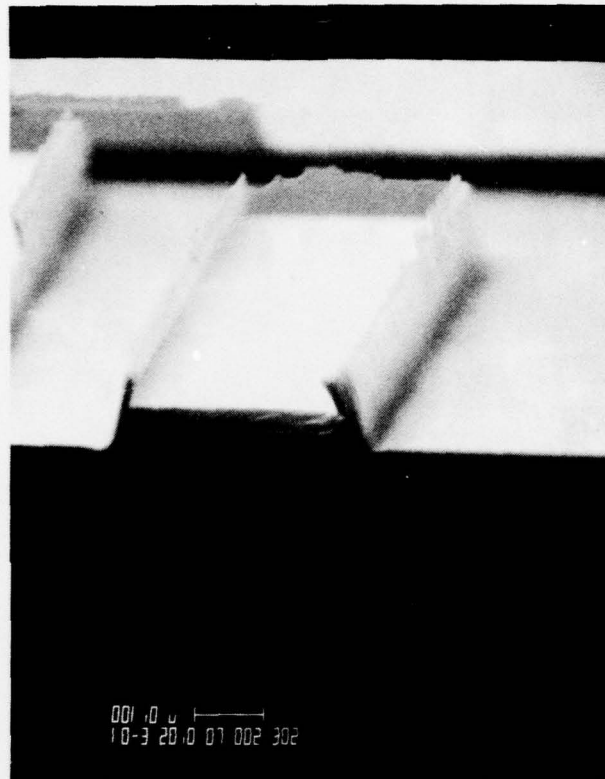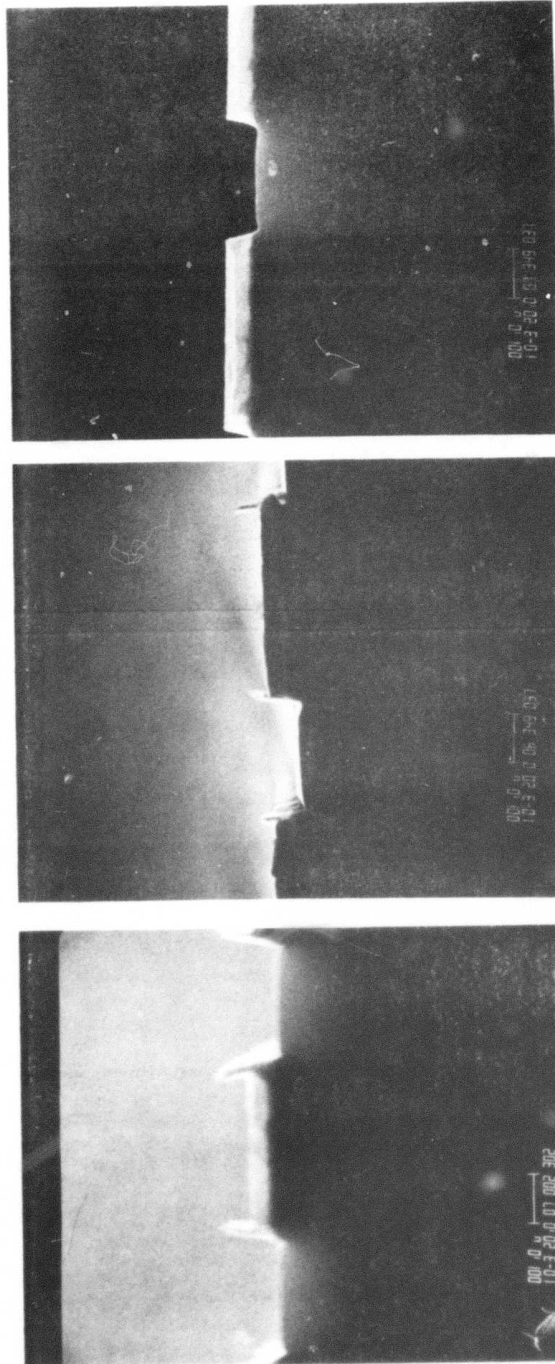Fig. 3.2-1 Scanning electron micrograph of the ridges formed by
redeposition. The incidence angle of the ion beam
was 90°.

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(a)

(b)

(c)

Fig. 3.2-2 Experimental results of ion beam etching of 300 Å Ti/5000 Å Au at various incidence angle θ. (a) $\theta = 90°$, (b) $\theta = 80°$, (c) $\theta = 70°$.

(θ = 90°, 80°, 70°). The sample rotates while it is being milled, so that all the sides of the holes are exposed to the beam. The figures show that the ridge height of the redeposited material decreases with increasing tilting of the beam angle. At an incidence angle of 70° there is no redeposited ridge and the etched pattern has a reasonable vertical edge.

A 70° incidence angle is a good compromise. It eliminates redeposition effects, and although the differential etch rate for Au and Si_3N_4 is no longer maximum at this angle, it is still acceptable. As shown in Fig. 3.2-3 from Quarterly Technical Report No. 6,[4] the Au etch rate at 70° is lower than its maximum value at θ = 90°, but the Si_3N_4 etch rate is still at its minimum value.

At this point the status of the ion milling process should be considered quite satisfactory but further refinements are still possible. In particular, work toward development of some reliable end-point detection methods, such as mass spectroscopy, is under consideration.
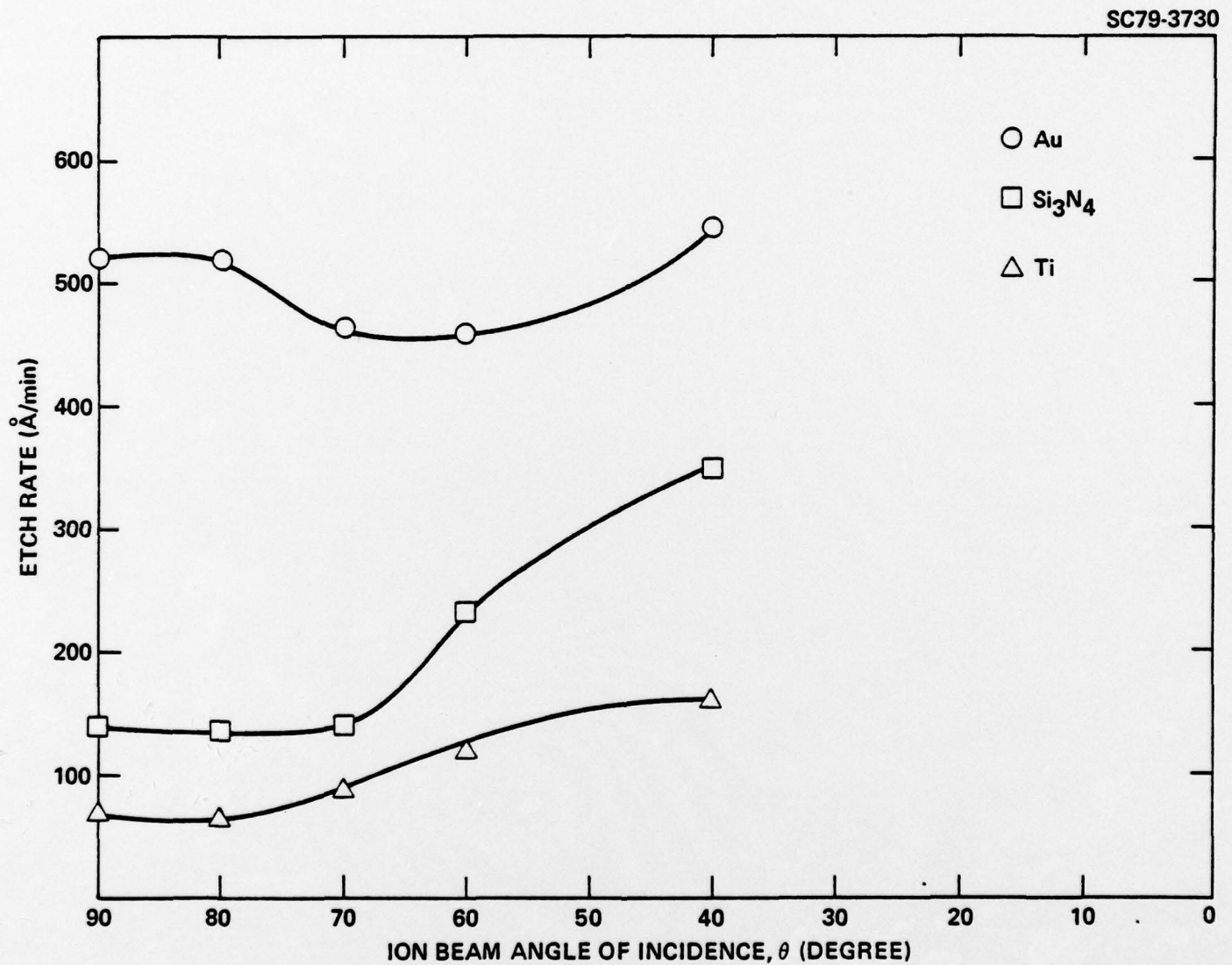
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Fig. 3.2-3 Etch rate vs. angle for 800V argon ion beam milling
(from Ref. 3).

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4.0 CIRCUIT PERFORMANCE

Evaluation of processed wafers using the automatic test system has continued on a routine basis, as a complementary step in the fabrication process. Doping profiles are also measured on chip by the automatic test system using the C-V technique.[1] A successful measurement of mobility profiles was recently accomplished using a "fat FET" configuration. The technique will be described, and results will be presented in Sec. 4.1. In Sec. 4.2 the strategy for testing the new 3 x 3 parallel multiplier circuits on wafers fabricated with mask set AR3 will be discussed. Finally, in Sec. 4.3, further refinements of the FET analytical model will be presented.

4.1   Low Frequency Measurements (Electronics Research Center)

Although the automatic collection of a large number of data from test devices on every wafer being processed and their statistical analysis provide sufficient information for monitoring and evaluating the results of the process, it is of great interest to obtain direct data on the properties of the implanted areas. This information is particularly important for the FET channel regions which determine the device characteristics, the pinchoff voltage being one of the most critical parameters. For this reason the measurement of carrier concentration profiles by the C-V technique has been implemented on our automatic measurement system,[1] and carrier concentration profiles are measured on chip for every wafer being processed. It is also of some interest to obtain profiles for the mobility which affects another

critical FET parameter, the transconductance. A measurement technique for drift mobility profiles has been implemented, and it is discussed in this section.

The standard Hall mobility measurements were considered impractical for two reasons, the first one being the requirement for a magnetic field perpendicular to the wafer, a requirement virtually incompatible with an automatic prober configuration. Secondly, a Hall measurement yields only average values for the mobility unless a stripping technique (differential Hall measurement), impractical for fabricated wafers is used. The technique chosen makes use of a "fat FET" structure, so called because it makes use of an FET device with a very large gate. In our test patterns the dimensions of the gate are 352 x 284 µm, on masks AR1 and AR2, and 145 x 350 µm on mask AR3. This test pattern is also used for the C-V measurements, treating the gate as the Schottky diode, and the source and drain (connected together) as the ohmic contact.

The principle behind the mobility profile measurement is illustrated in Fig. 4.1-1. The technique combines a C-V measurement with a measurement of channel conductance (or more precisely transconductance) as a function of gate voltage. After the charge density profile in the channel is calculated from the C-V profile, the measurements of channel conductance yield the mobility profile.[5,6] The equations governing the measurement are written on Fig. 4.1-1. The first equation expresses the channel conductance G as a function of the channel charge density ρ and the mobility μ, both functions of the depth w. Z is the gate width, and L is the gate length. The second

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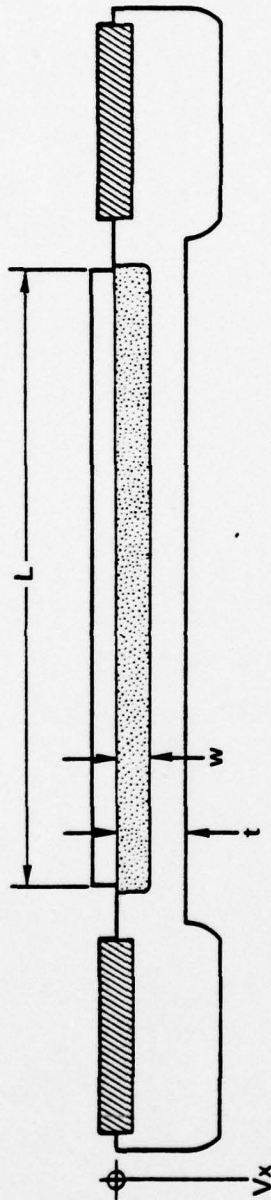
$$G = \frac{Z}{L} \int_w^t \rho(x)\mu(x)dx$$

$$V_g + V_{Bi} = \frac{1}{\epsilon} \int_w^0 dx \int_w^x \rho(x')dx'$$

FROM $\frac{\partial G}{\partial w}$ AND $\frac{\partial V_g}{\partial w}$

$$\frac{\partial G}{\partial V_g} = -\frac{Z}{L}\mu(w)\frac{\epsilon}{w}$$

FROM $g_m = \frac{\partial G}{\partial V_g} V_d$

$$\mu(w) = -\frac{Lwg_m(w)}{Z\epsilon V_d}$$

$$v_d \to 0$$

Fig. 4.1-1 Model for the calculation of the mobility profile from a "giant" FET test structure.

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equation, resulting from the integration of Poisson's equation, relates the gate voltage to the charge density under the gate. The derivation process, illustrated in Fig. 4.1-1, leads to the final equation for the mobility μ as a function of depth w. Note that the device transconductance g_m which appears in the equation must be measured in the linear region of the device, for a very small drain voltage V_d. It is necessary to keep the electric field in the channel as small as possible ($V_d \rightarrow 0$) so that the depletion layer width w does not vary appreciably from source to drain.

In order to apply the technique illustrated in Fig. 4.1-1, the carrier concentration profile is first measured by the standard C-V procedure. After this measurement, the FET characteristics are measured with a curve tracer *operating on its most* sensitive drain voltage range, obtaining the drain current as a function of gate voltage for a drain voltage of 0.05 V. For each value of gate voltage the depletion layer width w is calculated from the capacitance, and used in conjunction with the transconductance to calculate the mobility. An example showing the result of the measurement is given in Fig. 4.1-2 where the calculated mobility profile was superimposed on the automatic plot of the carrier concentration profile.

The mobility profile for a typical wafer shown in Fig. 4.1-2 reaches a channel mobility above 4000 cm^2/Vs. This is a quite satisfactory value, in agreement with mobility measurements on implanted layers on parallel chips. The mobility in Fig. 4.1-2 increases from the surface corresponding to the reduction of donor concentration.
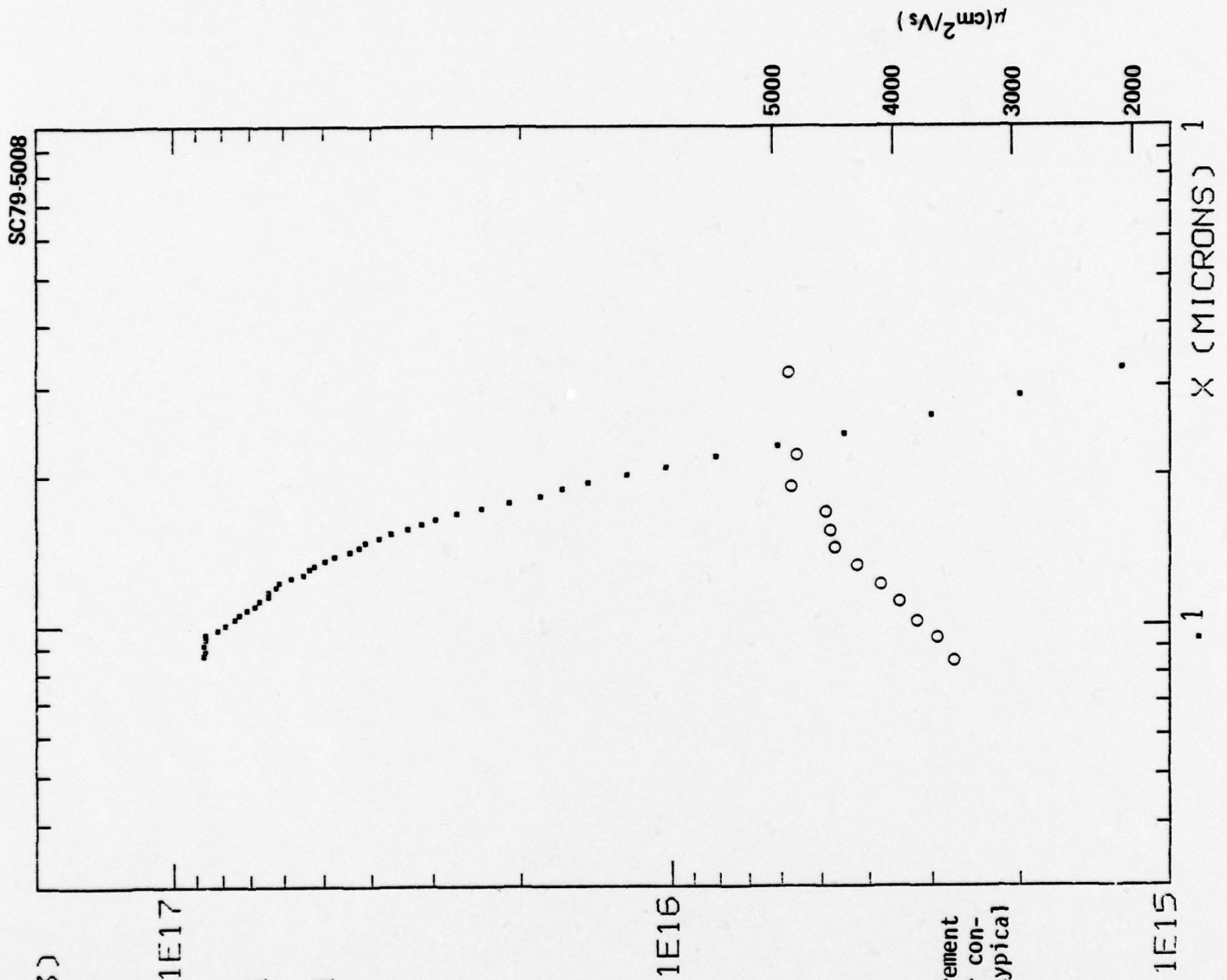
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Fig. 4.1-2 Result of an on-chip measurement of mobility and the carrier concentration profiles for a typical FET channel region.

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Although the mobility values reported in this section correspond to data from one wafer, and extensive mobility measurements were not made, the data reported here are representative of the FET channel mobility for most processed wafers. This statement is supported from Fig. 4.1-3 which displays the wafer average saturation current versus the wafer average pinchoff voltage for the 72 50 μm x 1 μm test FETs in test area T2, for a fairly large number of wafers processed under this program. The points on Fig. 4.1-2 are very strongly correlated following a curve passing through the origin. The strong correlation shown in the figure would not be possible if there were large mobility differences between wafers because mobility variations cause devices with the same pinchoff voltage to have different saturation currents. The data points for high pinch-off voltage are probably not very significant in this discussion because the saturation current for those devices is determined to some extent by velocity saturation, but strong correlation exists equally well for the wafer with low pinch-off voltage, where the devices follow a pure Shockley behavior.

Mobility profile measurements such as the one described above will be performed at times to continue sampling the characteristics of the implanted layers.

4.2   High Speed Testing (Electronics Research Center)

During the past quarter, preparations were made for the evaluation of the 3 x 3 parallel multiplier on mask set AR3. This circuit, containing 75 gates, was implemented with half adders and full adders as described in the
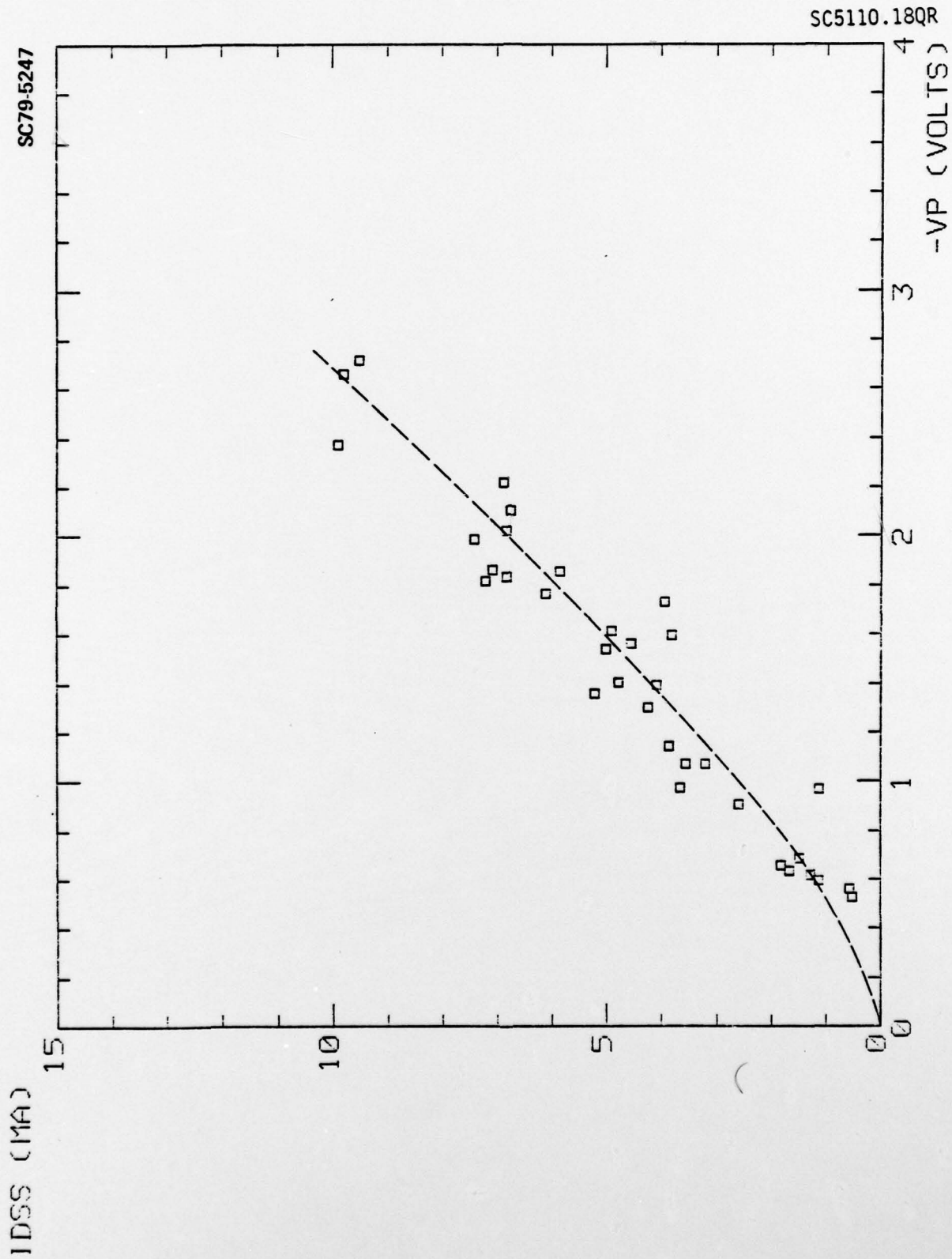
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Fig. 4.1-3 Average saturation current vs average pinchoff voltage of 50 x 1 μm FETs on test areas T2 for a number of processed wafers.

7th Quarterly Report.[1] A block diagram of the multiplier is shown in
Fig. 4.2-1.

Testing of the multiplier has been organized along three paths. Low
speed evaluation is being carried out on the Electroglas probe station using a
probe card to determine overall functionality of the circuit. Two approaches
are being utilized for this evaluation. The simplest technique biases all of
the multiplier inputs except for one at a fixed dc level (ground = logical
"0", V_{dd} = logical "1"). The remaining input is driven by a pulse generator
and outputs are examined for the proper logic state under these specific input
conditions. This mode is convenient for setting operating biases and for
evaluation of a few input code possibilities, but is would be very time
consuming to test all 64 possible input combinations by this approach.
Therefore, once functionality is established, an automatic data acquisition
system, utilizing an Analog Devices "MACSYM II" laboratory computer, will test
the circuit for all possible input code combinations, read the six output
lines for each test, and compare with the expected output. Test data files
will be stored on disc permitting further analysis of results. Results can be
sorted by the system to correlate errors for specific input codes.

This technique will allow complete functional evaluation of the 3 x 3
multiplier. Even though functional evaluation could be accomplished manually
at this level of complexity, it would be highly impractical to test future
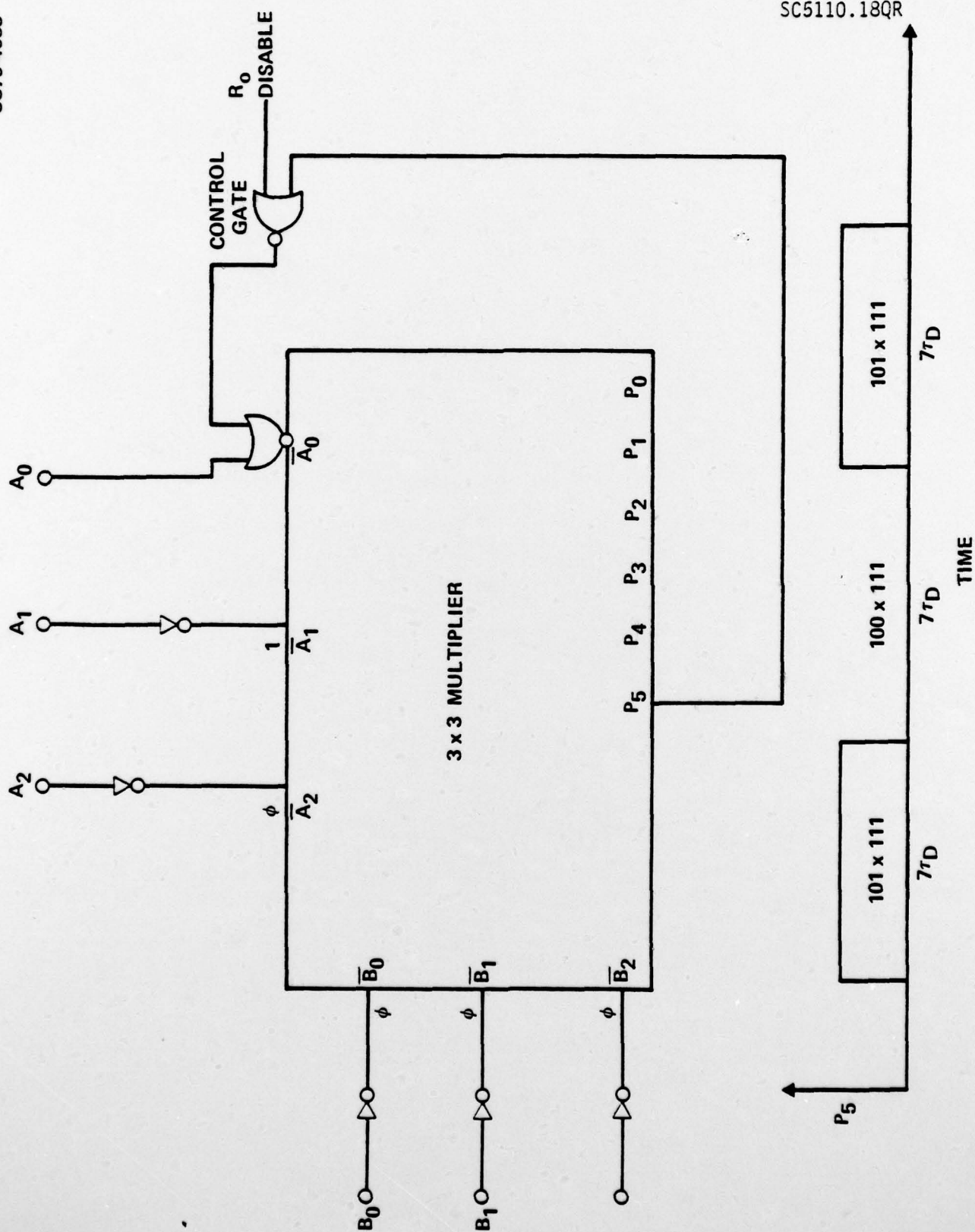multipliers (up to 8 x 8) without computer aided test capability.

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Fig. 4.2-1 Block diagram of a ring oscillator-like multiplexer and its output waveform (from Ref. 1).

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High speed testing will be carried out on the high speed probe station using the ring oscillator feedback mode, available on-chip (see Fig. 4.2-1). An additional NOR gate provides this feedback loop from the most significant product bit (P_5) to one of the least significant (A_0) input bits. By presetting the multiplier $B_2B_1B_0$ to 111 and the multiplicand $A_2A_1A_0$ to 100, the "0" output state of P_5 will be inverted, and will set A_0 to "1" then reversing the process. This produces an oscillation frequency of $1/14 \; \tau_d$.

During the next quarter, testing of the new AR3 wafers for multiplier operation will be completed.

4.3   GaAs FET Modeling (Cornell University)

During the past quarter, further modifications were implemented on the nonuniformly doped FET model[1] to include the effect of source resistance on the predicted I_{ds} vs V_{gs} and g_m vs V_{gs} characteristics. In addition, the model was adapted so that a modified Shockley (gradual channel approximation) model is utilized when the device reaches current saturation due to pinch-off rather than velocity saturation. In this non-velocity saturated region,

$$V_T + V_{gs} - I_{ds} R_s < V_s$$

where V_T is the pinch-off voltage referred to the device terminals, R_s is the source resistance and V_s the voltage drop across the portion of the channel under the gate at saturation. Above the limit of carrier velocity saturation,

the previously reported analytical model,[7,8] modified for nonuniform doping profile, was utilized.[1] Finally, for the case of low pinch-off devices typically used in digital logic applications, an ion implanted doping profile model was derived. This profile approximately reconstructs the doping distribution close to the surface by fitting N_d-N_a from C-V data measured on the doping tail.

The above modifications have resulted in much improved agreement with experimental FET data, particularly for higher pinch-off devices. Figure 4.3-1 shows the calculated and experimental g_m vs V_{gs} for a 50 μm wide FET with relatively high (-1.5V) pinch-off voltage. This was calculated by the non-hybridized saturation model without including source resistance.[1] Figure 4.3-2 also presents the transconductance g_m, this time for the modified model. Curve 4 represents experimental data while curve 1 represents the nonuniform profile calculation with R_s, curve 2 represents the nonuniform profile without R_s and curve 3 the uniform profile without R_s. Also, Fig. 4.3-3 presents I_{ds} vs V_{gs} for the same profile and model variations. As can be seen from the two figures, the nonuniform hybridized model with source resistance (curve 1) provides the best agreement with the experimental results. All factors seem to be essential in providing this agreement (R_s, nonuniform doping, and the transition to the Shockley model at low V_{gs}).

The calculation was also carried out for a device with low pinch-off voltage (-0.6V). The estimated profile was reconstructed from doping information measured on the tail of the implant. Figures 4.3-4 and 4.3-5 present calculated vs experimental data on the transconductance and drain-
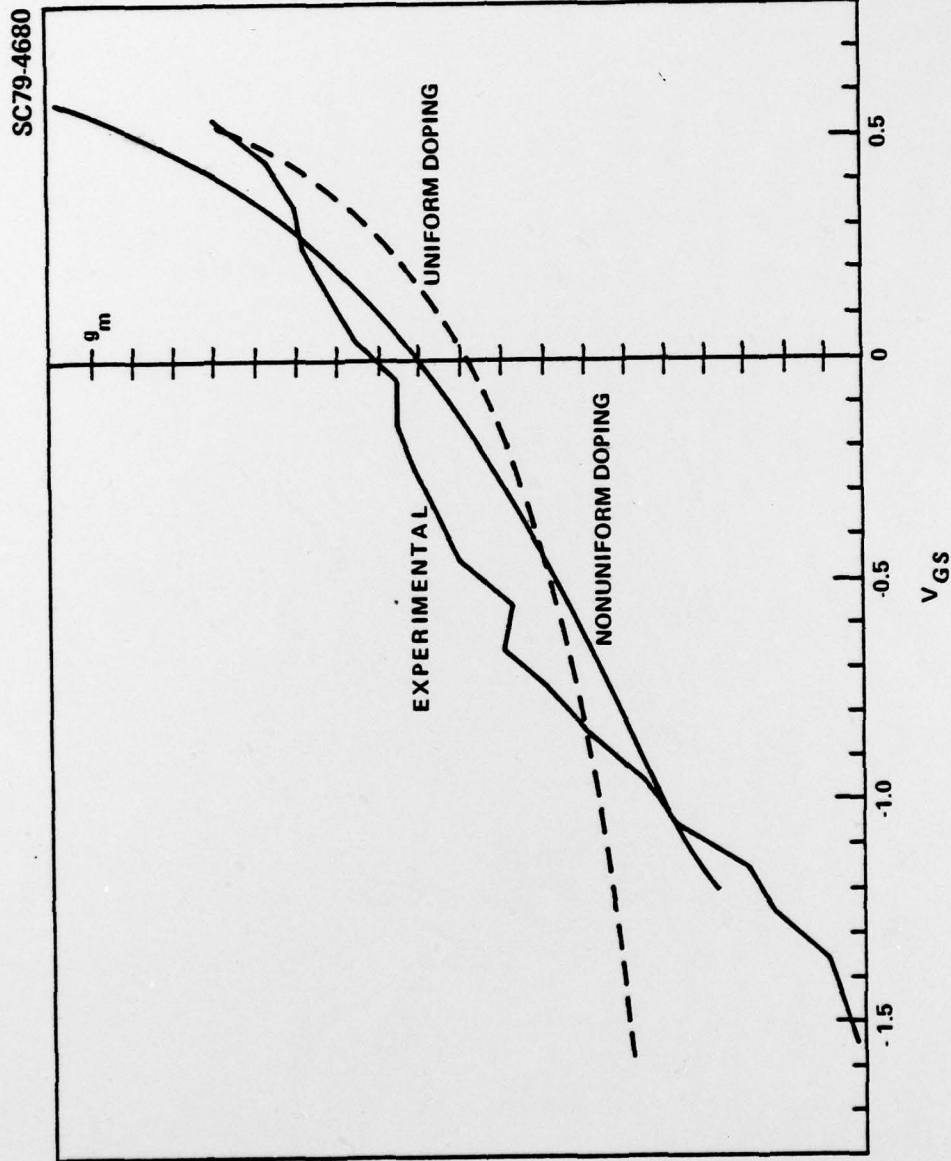
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Fig. 4.3-1 Transconductance as a function of gate-source voltage for a 50μm FET. Calculated transconductances are shown for both the uniform and non-uniform doping profiles (from Ref. 1).
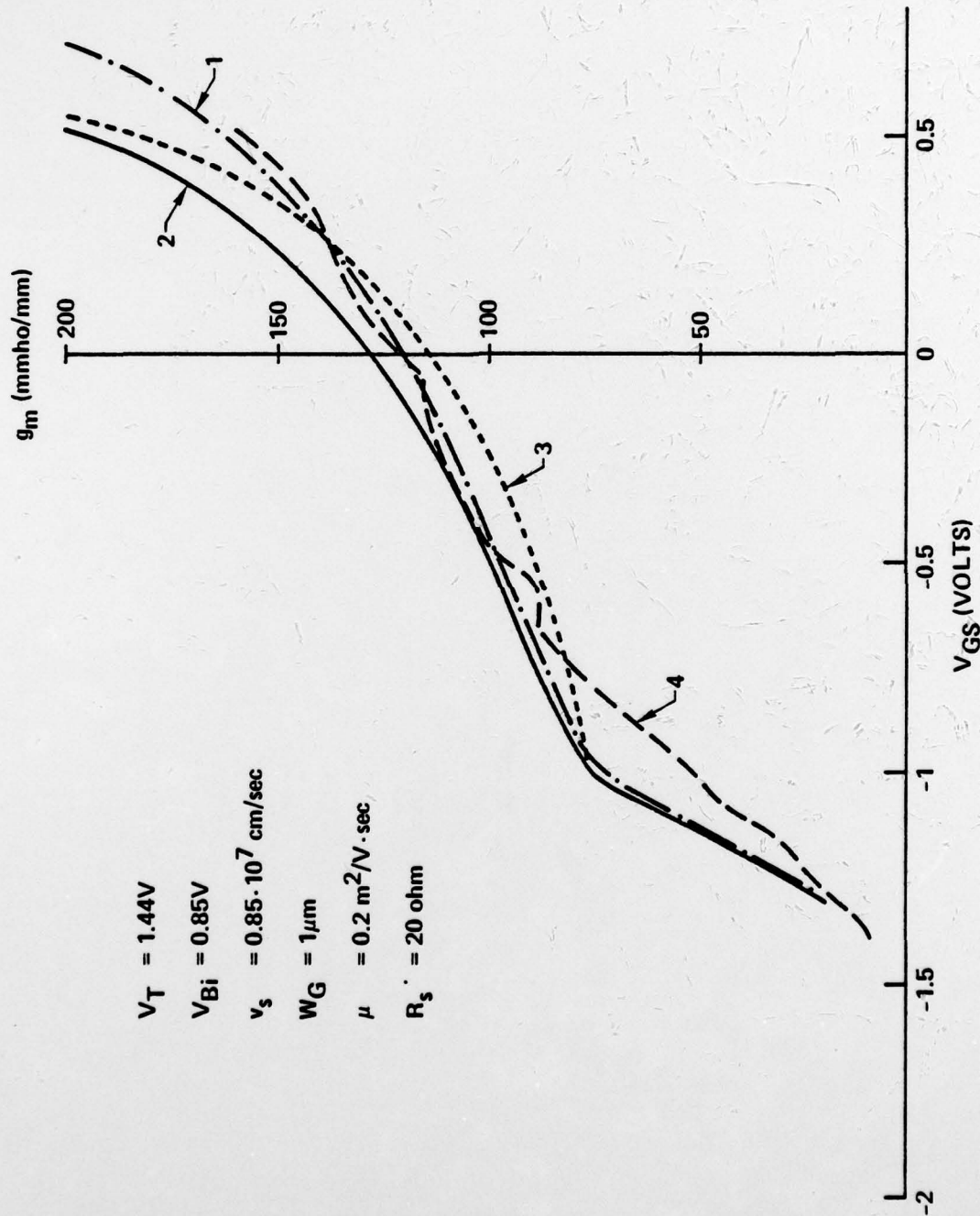
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$V_T = 1.44V$

$V_{Bi} = 0.85V$

$v_s = 0.85 \cdot 10^7$ cm/sec

$W_G = 1\mu m$

$\mu = 0.2$ m^2/V·sec

$R_s \cdot = 20$ ohm
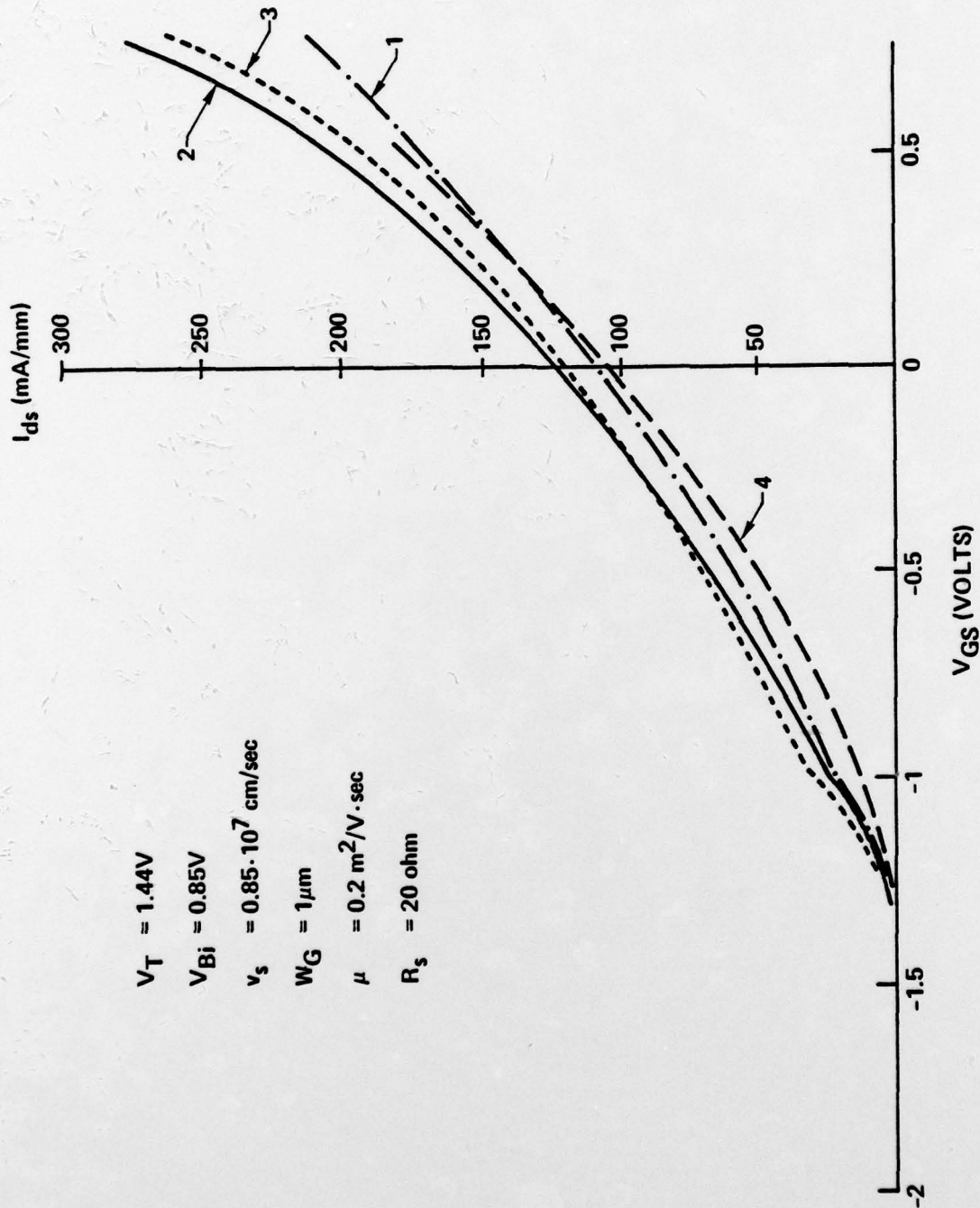
Fig. 4.3-2 Transconductance vs. gate-source voltage for a 50μm FET.
1. Non-uniform profile, R_s included; 2. Non-uniform profile,
R_s not included; 3. Flat profile, R_s not included;
4. Experimental data.

I_{ds} (mA/mm)

V_{GS} (VOLTS)

V_T = 1.44V

V_{Bi} = 0.85V

v_s = 0.85·10^7 cm/sec

W_G = 1μm

μ = 0.2 m^2/V·sec

R_s = 20 ohm

Fig. 4.3-3 Saturation current vs. gate-source voltage for a 50μm FET.
1. Non-uniform profile, R_s included; 2. Non-uniform profile,
R_s not included; 3. Flat profile, R_s not included;
4. Experimental data.

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g_m (mmho/mm)

V_T = 0.7V

V_{Bi} = 0.85V

v_s = $0.85 \cdot 10^7$ cm/sec

W_G = 1μm

μ = 0.2 m²/V·sec
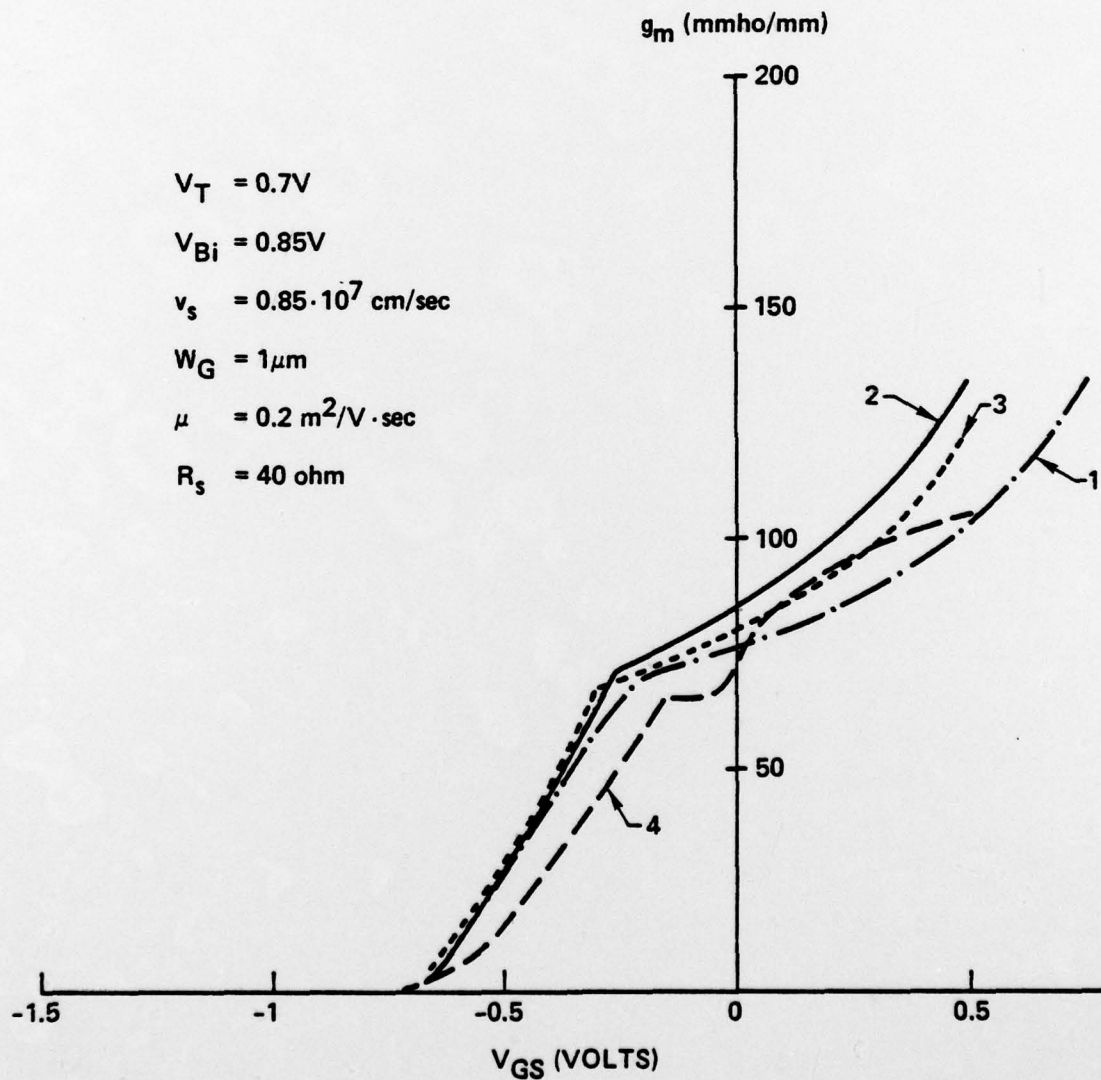
R_s = 40 ohm

V_GS (VOLTS)

Fig. 4.3-4 Transconductance vs. gate-source voltage for a low-pinchoff
            voltage 50μm FET. 1. Non-uniform profile, R_s included;
            2. Non-uniform profile, R_s not included; 3. Flat profile,
            R_s not included; 4. Experimental data.
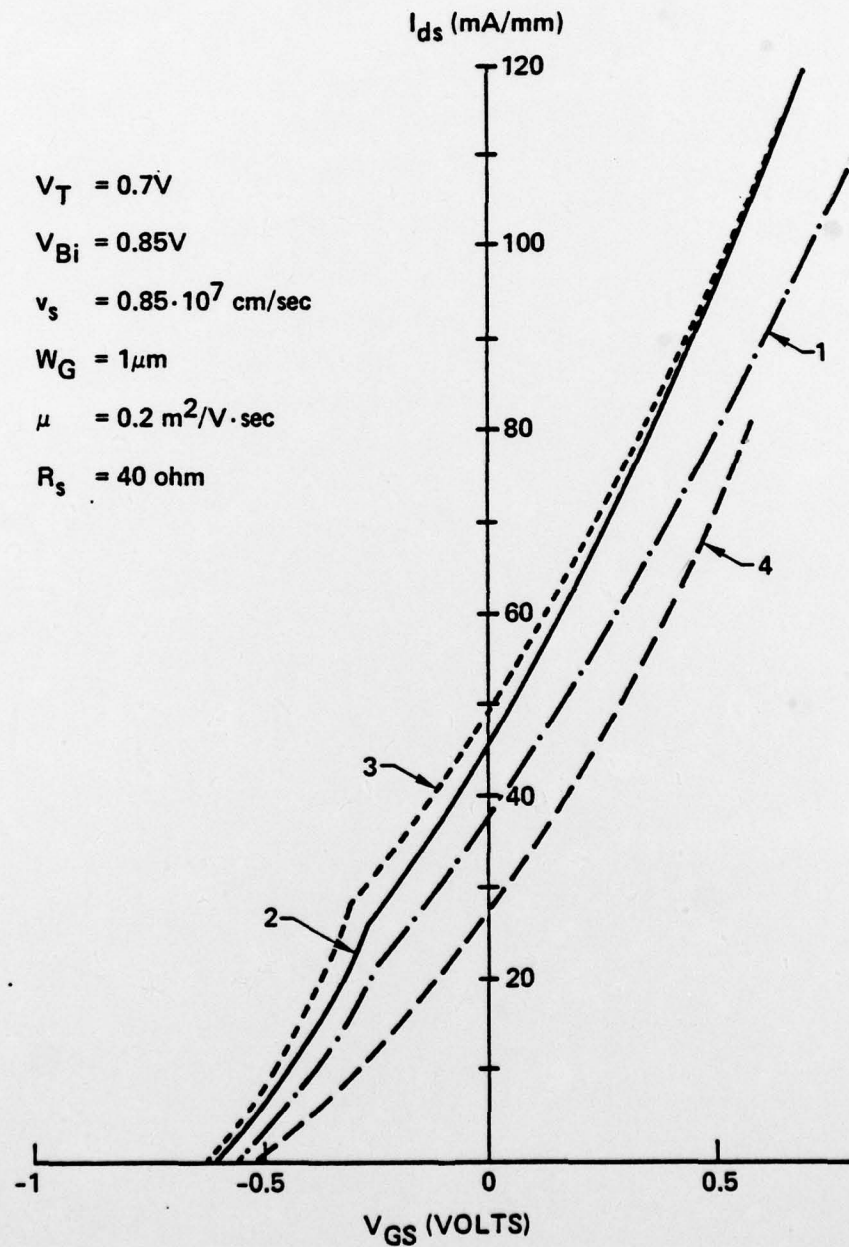
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I_ds (mA/mm)

V_T = 0.7V

V_{Bi} = 0.85V

v_s = 0.85·10^7 cm/sec

W_G = 1μm

μ = 0.2 m^2/V·sec

R_s = 40 ohm

V_GS (VOLTS)

Fig. 4.3-5 Saturation current vs. gate-source voltage for a low-pinchoff
voltage 50μm FET. 1. Non-uniform profile, R_s included;
2. Non-uniform profile, R_s not included; 3. Flat profile,
R_s not included; 4. Experimental data.

source current as a functions of V_{gs}. The same model variations were used on these plots as were discussed above. Here, the agreement is not quite as good, with a tendency for the calculated I_{ds} to exceed the experimental I_{ds}. This may indicate a smaller effective saturation velocity compared to the higher pinch-off case, or a greater dependence of the effective velocity on the voltage across the channel. Further variation of model parameters will be explored in order to improve the fit.

Additional comparisons of experimental data and dc characteristics calculated by this model will be explored at Rockwell during the next quarter. Efforts will be made to incorporate the improved nonuniform FET model in the low frequency automatic test software.

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This report covers the third quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The overall objective of this program is the development of a manufacturable process for high-speed low-power GaAs logic circuits. The goal for Phase I was to establish the technology, and demonstrate its viability by fabricating circuits reaching MSI complexity. The goal for Phase II is to achieve the capability of fabricating GaAs ICs of LSI complexity. The program involves the Rockwell International Electronics Research Center and three subcontractors: Cal Tech, Cornell University, and

Unclassified

Crystal Specialties, Inc.

The most important aspects of the work carried out in this quarter were the gaining of further insight into the causes for conversion of unqualified GaAs substrates, the fabrication of wafers with mask set AR3, and the preparation for evaluating the 3 x 3 parallel multiplier, a new circuit on AR3. This circuit will provide vital information for the design of the more complex circuits, on mask set AR4.

Work on all aspects of the program has continued. Evaluation (by SIMS) of the redistribution of Cr during annealing done on several different annealing caps indicate a dependence of the Cr profile on the As vacancy concentration. In addition, electrical evaluation of doping tails on Se implanted layers in unqualified substrates resulted in shallow donor and Cr profiles which have correlated well with bulk Cr density profiles obtained from SIMS data. The results support our model, which attributes the formation of an n-type layer after annealing of unqualified substrates to lack of compensation due to Cr depletion. As a result of the Cr redistribution analysis, efforts were initiated at Crystal Specialties to reduce the background donor concentration in the bulk material.

Optimization of the ion milling process for second level metal definition has continued. Etch rate and redeposition effects as a function of the angle of incidence have been evaluated. As a result, the ion milling method has been successfully used to fabricate wafers from mask sets AR2 and AR3 with excellent results, and it has replaced lift-off for the second level metallizations.

Acquisition of capacitance-voltage profiles and calculation of doping profiles from PM test patterns has been carried out automatically on the low frequency probe station. Mobility profiles, using a "fat FET" test pattern on PM, have also been measured, obtaining peak mobilities in excess of 4000 cm^2/Vs.

As mentioned above, a number of wafers have been processed using mask set AR3 during the past quarter. Several wafers are presently being evaluated for high speed performance of MSI circuits. The 3 x 3 parallel multiplier containing 75 gates is the first new MSI circuit being tested. Automatic data acquisition methods will be used to evaluate the functional accuracy of this circuit under all combinations of input codes at low speeds. Propagation delay times will be evaluated using the ring oscillator feedback mode of this circuit.

The FET device modeling work at Cornell has been extended to include the shape of the ion implanted doping profile. It has also been hybridized with the Schockly model to improve the fit with experimentally determined I-V characteristics near threshold.